posed in a second surface portion of the channel layer, which is opposite to a corresponding second conductive type region, and having an impurity concentration higher than the channel layer; a gate insulation film disposed on the channel layer; a gate electrode disposed on the gate insulation film; a surface electrode disposed on the channel layer; a backside electrode disposed on the substrate opposite to the super junction structure; and an embedded second conductive type region. A current flows between the surface electrode and the backside electrode. The embedded second conductive type region is disposed in a corresponding second conductive type region, protrudes into the channel layer, and contacts the contact second conductive type region. The embedded second conductive type region has an impurity concentration higher than the channel layer, and has a maximum impurity concentration at a position in the corresponding second conductive type region.

[0014] In the above semiconductor, the electric field easily concentrates around the embedded second conductive type region. Thus, a breakdown easily occurs around the embedded second conductive type region. Accordingly, an avalanche current easily flows from the embedded second conductive type region to the contact second conductive type region, so that an avalanche resistance is improved.

[0015] According to a second aspect of the present disclosure, a method for manufacturing a semiconductor device includes: forming a first conductive type region film on a substrate having a first conductive type; forming a plurality of first trenches on the first conductive type region film to reach the substrate so that the first conductive type region film is divided into a plurality of first conductive type regions, which are separated from each other with the first trenches; filling each first trench with a second conductive type region film; polishing a surface of the second conductive type region film so that the second conductive type region film is divided into a plurality of second conductive type regions, and the first conductive type regions and the second conductive type regions provide a super junction structure, wherein the first conductive type regions and the second conductive type regions extend in a first direction, and wherein the first conductive type regions and the second conductive type regions are alternatively arranged in a second direction; implanting a second conductive type impurity into the second conductive type regions; forming a channel layer having a second conductive type on the super junction structure; forming a plurality of second trenches to penetrate the channel layer and to reach a corresponding first conductive type region, wherein the second trenches have a stripe pattern; forming a gate insulation film on an inner wall of each second trench, and forming a gate electrode on the gate insulation film in each second trench, so that the second trenches, the gate insulation film and the gate electrode provide a trench gate structure; implanting a first conductive type impurity into a surface portion of the channel layer; implanting a second conductive type impurity into another surface portion of the channel layer; and heating the substrate so that the second conductive type impurity in the channel layer is diffused, and a contact second conductive type region is formed in the another surface portion of the channel layer, which is opposite to a corresponding second conductive type region. The contact second conductive type region has an impurity concentration higher than the channel layer. In the heating of the substrate, the first conductive type impurity in the channel layer is diffused, and a first conductive type layer is formed in the surface portion of the channel layer. The first conductive type layer has the first conductive type, and contacts a sidewall of a corresponding trench. In the heating of the substrate, the second conductive type impurity in the second conductive type regions is diffused, and an embedded second conductive type region is formed in a corresponding second conductive type region. The embedded second conductive type region has an end, which protrudes into the channel layer and contacts the contact second conductive type region. The embedded second conductive type region has the other end, which is deeper than a bottom of a corresponding trench. The embedded second conductive type region has an impurity concentration higher than the channel layer, and has a maximum impurity concentration at a position in the corresponding second conductive type region.

[0016] In the above method, the thermal treatment temperature is low, and the thermal treatment time is short. Thus, the charge balance between the first and second conductive type regions is not changed.

[0017] According to a third aspect of the present disclosure, a method for manufacturing a semiconductor device includes: forming a first conductive type region film on a substrate having a first conductive type; forming a plurality of first trenches on the first conductive type region film to reach the substrate so that the first conductive type region film is divided into a plurality of first conductive type regions, which are separated from each other with the first trenches; filling each first trench with a second conductive type region film, and forming the second conductive type region film on the first conductive type regions; implanting a second conductive type impurity into the second conductive type region film in each trench with using the second conductive type region film on the first conductive type regions as a mask; polishing a surface of the second conductive type region film so that the second conductive type region film is divided into a plurality of second conductive type regions, and the first conductive type regions and the second conductive type regions provide a super junction structure, wherein the first conductive type regions and the second conductive type regions extend in a first direction, and wherein the first conductive type regions and the second conductive type regions are alternatively arranged in a second direction; forming a channel layer having a second conductive type on the super junction structure; forming a plurality of second trenches to penetrate the channel layer and to reach a corresponding first conductive type region, wherein the second trenches have a stripe pattern; forming a gate insulation film on an inner wall of each second trench, and forming a gate electrode on the gate insulation film in each second trench, so that the second trenches, the gate insulation film and the gate electrode provide a trench gate structure; implanting a first conductive type impurity into a surface portion of the channel layer; implanting a second conductive type impurity into another surface portion of the channel layer; and heating the substrate so that the second conductive type impurity in the channel layer is diffused, and a contact second conductive type region is formed in the another surface portion of the channel layer, which is opposite to a corresponding second conductive type region. The contact second conductive type region has an impurity concentration higher than the channel layer. In the heating of the substrate, the first conductive type impurity in the channel layer is diffused, and a first conductive type layer is formed in the surface portion of the channel layer. The first conductive type layer has the first conductive type, and contacts a side-